Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) ~~Integrated~~ An integrated circuit comprising:

a plurality of modules (M) for processing applications, each having a local memory (LM);~~, said integrated circuit further comprising:~~

a global memory (GM), which can be shared by said plurality of modules (M);

interconnected data communications paths for interconnecting said modules (M) and said global memory (GM); and

~~one~~ a memory managing unit (MMU) being associated ~~to~~ with each of said modules (M), for determining whether said local memory (LM) provides sufficient memory space for processing ~~the~~ a currently processed application on one of the plurality of modules (M) and for in response to the determining that there is not sufficient memory space, ~~requesting~~ issuing a reservation request for memory space within a global buffer (FB) in said global memory (GM) to be exclusively reserved for ~~the~~ processing data of ~~the associated module~~ the one of the plurality of modules ~~(M)~~ and for in response to the determining that there is not sufficient memory space, ~~requesting~~ issuing a path request for a dedicated communication path between the ~~associated module~~one of the plurality of modules and the global buffer.

2. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein said communication path having communication properties according to the ~~required access to the global memory (GM)~~path request.

3. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, further comprising a resource managing unit (RMU) for allocating memory space in said global memory (GM) according to the reservation ~~_~~request of said memory managing unit (MMU).

4. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 3, wherein said resource managing unit (RMU) is adapted for setting a communication path based on communication properties as requested by said memory managing unit (MMU).

5. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 4, further comprising an address translation unit (ATU) associated ~~to~~ with each of said modules (M) for performing an address translation for data of an application, which data are stored in said global buffer (FB) in said global memory (GM).

6. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 3, wherein said resource managing unit (RMU) is adapted to perform an access arbitration for said global memory (GM).

7. (Currently Amended) ~~Integrated~~ The integrated circuit according to claim 1, wherein said local memory (LM) comprises a prefetch buffer (PB) for prefetching data from said global buffer (FB).

8. (Currently Amended) ~~Method~~ A method for memory allocation in an integrated circuit comprising a plurality of modules (M) for processing applications, wherein each module comprises a local memory (LM), a global memory (GM) being adapted to be shared between said plurality of modules (M), ~~comprising the steps of~~ the method comprising:

~~memory managing by~~ determining whether said local memory (LM) provides sufficient memory space for processing a currently processed application of the one of the plurality of modules;

~~and for~~ in response to the determining that there is not sufficient memory space, ~~requesting~~ issuing a reservation request for memory space within a global buffer (FB) in said global memory (GM) to be exclusively reserved for processing data of the one of the plurality of modules ~~one of said modules (M)~~ and ~~for,~~ in response to the determining that there is not sufficient memory space, ~~requesting~~ issuing a path request for a dedicated communication path between the one of the plurality of modules~~associated module~~ and

the global buffer.~~, when there is not sufficient memory space available in said local memory (LM)~~

9. (Currently Amended) The integrated circuit of claim 3, wherein the RMU allocates memory space in said global memory in response to determining that there is adequate space in the global memory to support the reservation request and in response to determining that there is adequate transmission bandwidth to support the path request.

10. (Previously Presented) The integrated circuit of claim 1, wherein the MMU determines whether the LM provides sufficient memory space for the currently processed application by comparing the memory space in the LM to a predetermined value.

11. (Currently Amended) The integrated circuit of claim 3, wherein the RMU provides an address of the global buffer to the MMU and wherein the MMU uses the provided address to perform address translation between an address provided by the one of the plurality of modules ~~associated module~~ to the address of the global buffer.